PAPER

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Optimized multi-step synchronous electric charge extraction via accurate electrical efficiency analysis

Hao Tang[1,2], Weiqun Liu[1,*], Guobiao Hu[2], Jian Liu[3] and Dawei Dong[1]

[1] School of Mechanical Engineering, Southwest Jiaotong University, Chengdu 610031, People's Republic of China
[2] Internet of Things Thrust, The Hong Kong University of Science and Technology (Guangzhou), Guangzhou 511400, People's Republic of China
[3] State Grid Jiangsu Electric Power Co Ltd Research Institute, Nanjing 211103, People's Republic of China

E-mail: weiqunliu@home.swjtu.edu.cn

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Abstract

The synchronous electric charge extraction (SECE) circuit has been widely used for piezoelectric energy harvesting due to its load independence properties but suffers from low circuit quality. In recent years, the multi-step (MS) energy extraction strategy has been proposed to reduce electrical dissipation. To offer deeper insights into how the MS strategy improves electrical efficiency and thereby maximizes the potential capacity of the SECE circuit, a theoretical model is developed to analyze the energy flows at the synchronous instants. Based on the theoretical model, the optimal voltage-flip sequences (VFSs) for two-step (2S) and three-step (3S) SECE circuits are determined. Moreover, this method is further extended to a general N-step case using a recursive approach. Good agreement between the experimental and the theoretical results has validated the proposed optimal VFSs. Compared to the standard SECE circuit, the 2S-SECE and 3S-SECE circuits can enhance efficiency by 41.9% and 65.5%, respectively, at an initial voltage of 2.5 V, and harvest additional power of 352 μW and 568 μW when the voltage increases to 40 V. The proposed VFSs provide a valuable reference for optimizing the performance of the MS-SECE circuit.

Keywords: piezoelectric energy harvesting, synchronous electric charge extraction, multi-step energy extraction, electrical efficiency, optimal voltage-flip sequence

1. Introduction

Piezoelectric vibration energy harvesting (PVEH) is a promising technique that can be an alternative to the traditional battery with the advantages of compactness, high power density, low cost, and, most importantly, renewability [1]. To improve the performance of PVEH devices, many solutions have been proposed to increase the power output and enlarge the working bandwidth from the structural design perspective [2–7]. On the other hand, many efforts have also been devoted to interface circuit design and optimization [8–12]. Using the standard energy harvesting circuit [13], which consists of a full-bridge rectifier and a filter capacitor, as the benchmark, nonlinear circuits, such as the parallel synchronous switching harvesting on inductor (SSHI) [14] and the serial-SHI [15] circuits, were proposed with the harvested power increased by several times. However, impedance matching is required for the SSHI techniques due to the direct connection between the piezoelectric element and the load [16, 17]. The later-developed synchronous electric charge extraction (SECE) circuit [18, 19] realizes load independence by separating the energy extraction process

* Author to whom any correspondence should be addressed.

into two phases, resulting in a 400% improvement under weak electromechanical coupling conditions.

The above-mentioned nonlinear interface circuits improve the performance of PVEH systems by introducing synchronous instants at the extremums of mechanical displacement. This modification effectively prevents energy backflow and enhances the energy extracted from the piezoelectric element by ensuring that the piezoelectric voltage is always in phase with the equivalent current [20]. However, considerable energy is dissipated due to parasitic resistance in the LC oscillation loop during synchronous instants. The unavoidable electrical dissipation dramatically hinders the electrical efficiency and diminishes the benefits of those nonlinear circuits.

Using high-quality components, especially inductors, can improve electrical efficiency to some extent, but the cost and the required space will significantly increase. The multi-step energy extraction (MSEE) technology is therefore proposed to divide the energy extraction process into several successive phases, thereby reducing the RMS value of the current and minimizing resistive dissipation. Liang and Chung [21] proposed a synchronized multiple bias-flip interface circuit based on the SSHI topology and studied the optimal bias-flip strategy. Based on this concept, a parallel synchronized triple bias-flip (P-S3BF) circuit was proposed and implemented using six MOSFET switches [22, 23]. Similarly, the series counterpart of P-S3BF, known as the S-S3BF circuit, was also developed using a similar implementation [24, 25]. However, extra topology design, more biased voltage sources, and complicated control signals are required for the above SSHI-based multi-step synchronous switching circuits.

In contrast, the MSEE technique can be more easily applied to the SECE topology by a few switch actions. Teng *et al* [26] proposed a multiple charge extraction and bias-flipping circuit to increase extracted and harvested power through several charge extraction phases and a bias-flipping phase at each synchronous instant. The MS-SECE circuit was also implemented on integrated circuit (IC) platform for a more compact size and higher electrical efficiency [27, 28], allowing for up to a 25% increase compared with traditional SECE circuits. Considering that the power extracted from the piezoelectric element by the SECE circuit remains constant once the initial voltage is determined, the MSEE strategy only benefits from enhanced electrical efficiency, which is closely dependent on the voltage-flip sequence (VFS) at the synchronous instants. In the aforementioned works, the piezoelectric energy is transferred through several successive discharges of the same energy segment for simplicity without detailed theoretical investigations. However, the optimal VFSs for MS-SECE circuits, referred to as the optimized MSEE strategy, are currently lacking. Therefore, a theoretical model that can predict the electrical efficiency of the MS-SECE circuit is urgently required to determine the optimal VFSs.

Unfortunately, early studies indicated that the performance of the SECE circuit is tied to the extracted energy from the piezoelectric element without addressing the harvested power or discussing electrical efficiency [18, 29]. To address this issue, Chen *et al* [30] revisited the joint dynamics and the harvested power of PVEH systems with the SECE circuit by using impedance modeling. Morel *et al* [31] proposed a unified model to evaluate the electrical efficiency of SECE circuits using the circuit quality factor and the voltage inversion ratio. Nevertheless, these methods may still misestimate the electrical efficiency since some assumptions are made for simplification during the analysis, and thus, fail to accurately predict the final harvested energy and the electrical efficiency of the SECE circuit.

Given the above research gap, the paper presents, for the first time, an accurate theoretical model for estimating the electrical efficiency of SECE circuits. Based on the electrical domain analysis, the model can numerically estimate every energy flow at the synchronous instants with more detailed parasitic effects considered. Specifically, it precisely describes the current behavior during the secondary working phase, allowing for an accurate evaluation of the corresponding energy dissipations, which were often simplified or neglected previously. Moreover, the model can be extended to evaluate the electrical efficiency of MS-SECE circuits. On this basis, the effectiveness of the MSEE strategy is studied in detail, and more importantly, the optimal VFSs for the MS-SECE circuit are determined.

The remaining part of this paper is organized as follows. Section 2 introduces the SECE circuit and MSEE strategy. The theoretical model of the MS-SECE circuit is established in section 3. In section 4, the electrical efficiency is analyzed, and the optimal VFS for the MS-SECE circuit is studied. Section 5 presents the experimental results and discussions. Finally, section 6 outlines the conclusions.

2. SECE circuit and MSEE strategy

Figure 1 shows an overview of the SECE circuit topology and the corresponding working waveforms. Focusing on the electrical domain to better investigate the electrical efficiency issue, the piezoelectric element is modeled as a current source in parallel with an intrinsic capacitance, C_p, as shown in figure 1(a). Figure 1(b) depicts the working waveforms of the piezoelectric voltage V_p, the load voltage V_{load}, and the mechanical displacement x. During the most time of the mechanical vibration period T_{ME}, the switch S is open, and V_p varies with x. At t_0 and $t_0 + T_{\text{ME}}/2$ moments, V_p and x reach their extremums, and V_p suddenly drops to zero by conducting the LC oscillations. The relationship between the magnitudes of piezoelectric voltage and mechanical displacement for the SECE circuit can be expressed as [29]

$$V_m = 2\frac{\alpha}{C_p}x_m \tag{1}$$

where α is the force factor-voltage factor and x_m is the displacement amplitude. Generally, the energy extraction process of the SECE circuit is completed by two stages via two different LC oscillations at each synchronous instant. As observed in figure 1(c), the primary stage transfers the electrostatic energy stored in C_p to the inductor L through the first LC oscillation, which is referred to as the energy transferring (ET) phase. When V_p drops to around zero, the secondary stage,

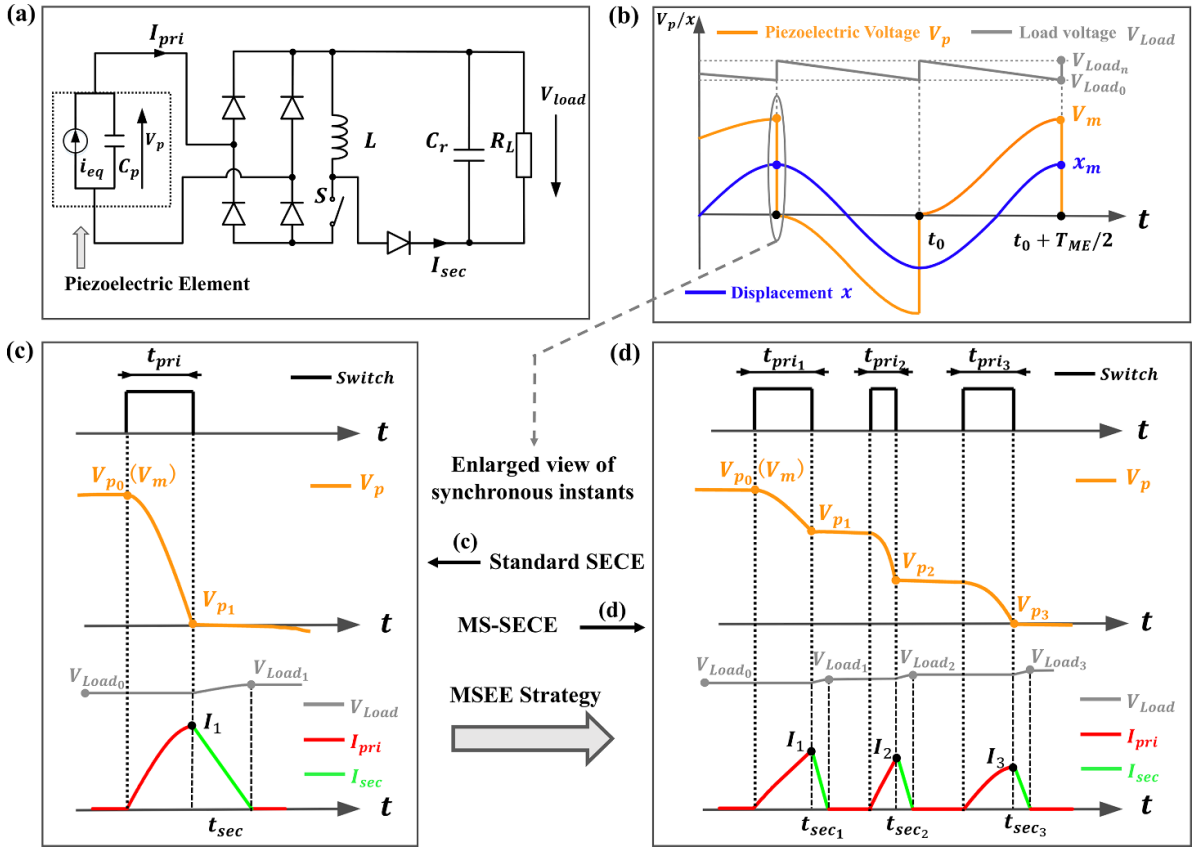

Figure 1. The topology and working waveforms of the SECE and MS-SECE circuits. (a) Circuit topology; (b) working waveforms; (c) the enlarged waveforms of the SECE circuit at the synchronous instants; (d) the enlarged waveforms of the MS-SECE circuit at the synchronous instants.

i.e. the energy charging (EC) phase, starts, and the freewheeling current charges the storage capacitor C_r through the second LC oscillation. Considering that the energy extraction process happens at both positive and negative extremums in one T_{ME}, the extracted power is expressed as

$$P_{\mathrm{ext}} = \frac{\omega}{\pi} E_{\mathrm{ext}} = \frac{\omega}{2\pi} C_p V_m^2. \tag{2}$$

The waveforms of the MS-SECE circuit at the synchronous instants are depicted in figure 1(d). By applying the MSEE strategy, the energy extraction process will alternate between the ET and EC phases, dividing the single-step process into several successive steps. It can be observed that the peaks of the synchronous current are reduced a lot for the MS-SECE circuit. Therefore, the electrical efficiency is enhanced as the electrical dissipation is reduced. Notably, the total extracted energy E_{ext} remains unchanged for the MS-SECE circuit since the start and the end voltages are exactly the same as those of the SECE circuit. Therefore, the working waveforms of the MS-SECE circuit are consistent with those in figure 1(b) since the synchronous instant is much shorter than T_{ME}. This phenomenon indicates that the MSEE strategy has little influence on the dynamics of the electromechanical system [9, 11]. In other words, the improved performance of the MSEE strategy benefits from the electrical domain, while the mechanical dynamics remain untouched. Therefore, the analysis of the MSEE strategy applied to the SECE circuit will focus on the electrical domain, placing particular emphasis on the initial voltage as the most crucial factor. In figure 1(d), the energy extraction process is divided into three steps, each consisting of an ET phase and an EC phase. V_{p_n} denotes the intermediate voltage, and I_n refers to the peak value of the synchronous current after the n^{th} ET phase; V_{load_n} is the load voltage on the storage capacitor C_r after the n^{th} EC phase.

As the intermediate voltage V_{p_n} directly correlates to the current peak values I_n, different combinations of V_{p_n}, i.e. the VFS, would result in different amounts of electrical dissipation energies in both ET and EC phases. In practice, the VFSs for the MS-SECE circuits can be directly controlled by setting specific switching control signals to the expected values. Therefore, the general optimal VFSs are desired to fully exploit the potential of the MSEE strategy on the SECE circuit. For this reason, a more detailed theoretical model is necessary to accurately evaluate the amounts of each energy flow and the electrical efficiencies of each working phase of the MS-SECE circuit.

3. Theoretical model

Figure 2 shows the circuit loops and energy flows of different phases in the SECE circuit. In the ET and EC loops, the energies are transferred by two different LC oscillations with

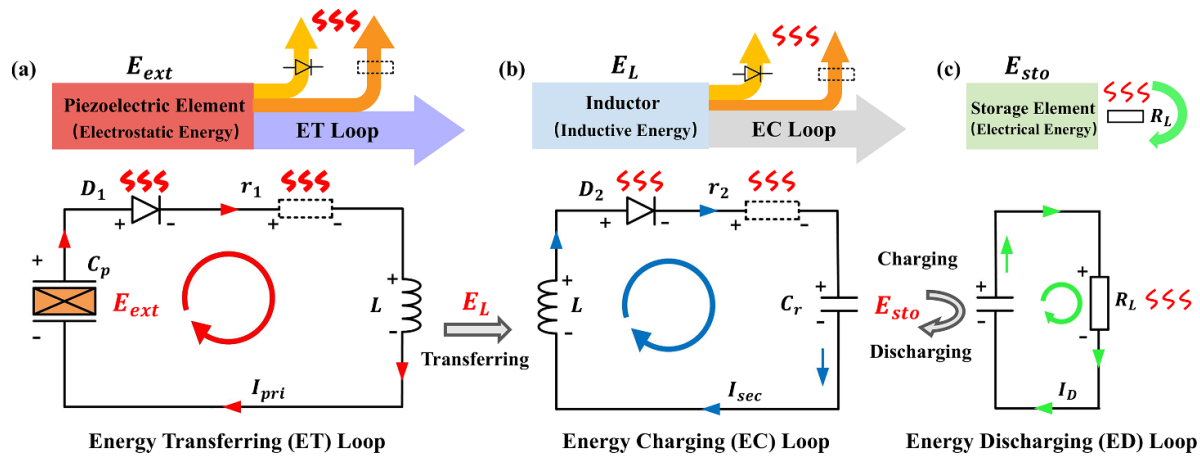

Figure 2. The circuit loops and energy flows at the synchronous instants. (a) The energy transferring loop; (b) the energy charging loop; (c) the energy discharging loop.

the help of the inductor. In this process, the voltage drops of diodes D_1, D_2 cause the diode dissipation, while the resistances r_1, r_2 are used to account for the parasitic resistive dissipation in the switches, inductor, lines, etc. In addition, an energy discharging (ED) loop is considered for the first time in our work, where the storage capacitor C_r and the load R_L will influence the electrical efficiency of the EC phases. In previous studies [18, 29], the electrical efficiency of the SECE circuit was neglected, as the energy extracted from the piezoelectric element was directly regarded as the harvested power [32]. The load independence of the SECE circuit implies the constant extracted power rather than the harvested power. The extracted power would remain constant if the electrical efficiency were not considered. In fact, the load R_L will influence the value of the load voltage V_{Load} in the steady state. On the other hand, V_{Load} serves as the initial condition in the differential equation of the EC loop, which in turn affects the behavior of the secondary synchronous current as well as the dissipations in the EC phases. Therefore, it is essential to include the ED loop for the accurate analysis of the electrical efficiencies. In particular, a theoretical model is presented with careful consideration of the energy flow relationships in all loops, enabling us to calculate the amount of each energy flow by numerically solving V_{Load} in the steady state for both SECE and MS-SECE circuits.

3.1. Energy transferring loop

The circuit loop and energy flow relationship of the ET phase is shown in figure 2(a). The piezoelectric voltage V_p and the primary synchronous current I_{pri} follows the governing equation of equation (3), where r_1 is the sum of parasitic resistance and V_{d1} is the voltage drop of the diode. For the n^{th} ET phase, considering the initial conditions $V_p(0) = V_{p_{n-1}}$ and $\dot{V}_p(0) = 0$, the expressions of V_p and I_{pri} can be described by equations (4) and (5),

$$L\ddot{V}_p + r_1\dot{V}_p + \frac{1}{C_p}V_p = \frac{V_{d1}}{C_p} \tag{3}$$

$$V_p(t) = \left(V_{p_{n-1}} - V_{d1}\right)\frac{1}{\sqrt{1-(1/2Q_I)^2}} \times \sin\left(\omega_{LC}\sqrt{1-(1/2Q_I)^2}t + \phi\right)\mathrm{e}^{-\frac{\omega_{LC}}{2Q_I}t} \tag{4}$$

$$I_{\text{pri}}(t) = \sqrt{C_p/L}\left(V_{p_{n-1}} - V_{d1}\right)\frac{1}{\sqrt{1-(1/2Q_I)^2}} \times \sin\left(\omega_{LC}\sqrt{1-(1/2Q_I)^2}t\right)\mathrm{e}^{-\frac{\omega_{LC}}{2Q_I}t} \tag{5}$$

$$\phi = \arcsin\left(\sqrt{1-\zeta_{LC}{}^2}\right); \zeta_{LC} = \frac{r_1}{2}\sqrt{C_p/L} = \frac{1}{2Q_I}; \omega_{LC} = \sqrt{1/LC_p} \tag{6}$$

where Q_I and ω_{LC} are the circuit quality factor and the natural angular frequency of the ET loop. The time period t_{pri_n} of the n^{th} ET phase can be numerically solved by equation (4) with the target intermediate voltages $V_{p_{n-1}}$ and V_{p_n}. The peak current I_n is calculated by equation (5). Subsequently, the dissipated energy $E_{d\_\text{pri}_n}$ in the n^{th} ET phase can be evaluated by equation (7). Clearly, the diode plays an important role in the circuit dissipation in addition to the serial resistance, especially when $V_{d1} > I_n r_1$. In consideration of the extracted energy and stored energy on the inductor. The energy flow relationship for the n^{th} ET phase can be described by equation (8),

$$E_{d\_\text{pri}_n} = E_{d\_\text{pri}\_r_n} + E_{d\_\text{pri}\_d_n} = \int_0^{t_{\text{pri}_n}} I_{\text{pri}}^2 r_1 \mathrm{d}t + \int_0^{t_{\text{pri}_n}} V_{d1} I_{\text{pri}} \mathrm{d}t \tag{7}$$

$$E_{\text{ext}_n} = \frac{1}{2}C_p\left(V_{p_{n-1}}^2 - V_{p_n}^2\right); E_{L_n} = \frac{1}{2}LI_n^2 = E_{\text{ext}_n} - E_{d\text{pri}_n} \tag{8}$$

where E_{ext_n} is the extracted energy and E_{L_n} represents the energy transferred to the inductor for the n^{th} ET phase.

3.2. Energy charging loop

The EC phase is dominated by another *LC* oscillation loop of L, r_2, D_2 and C_r as illustrated in figure 2(b). The behaviors of voltage and current can be described as

$$L\ddot{V}_{\mathrm{Load}} + r_2\dot{V}_{\mathrm{Load}} + \frac{1}{C_r}V_{\mathrm{Load}} = -\frac{V_{d2}}{C_r} \tag{9}$$

where V_{Load} is the steady-state load voltage. Solving equation (9), the V_{Load} and the secondary synchronous current I_{sec} can be expressed as

$$V_{\mathrm{Load}}(t) = A_n e^{\lambda_1 t} + B_n e^{\lambda_2 t} - V_{d2} \tag{10}$$

$$I_{\mathrm{sec}}(t) = C_r\left(A_n\lambda_1 e^{\lambda_1 t} + B_n\lambda_2 e^{\lambda_2 t}\right) \tag{11}$$

where λ_1 and λ_2 are the roots of the corresponding characteristic equation of equation (9), while A_n and B_n are the undetermined coefficients for the n^{th} EC phase. Given the initial conditions $V_{\mathrm{Load}}(0) = V_{\mathrm{Load}_{n-1}}$ and $\dot{V}_{\mathrm{Load}}(0) = I_n/C_r$, we have:

$$A_n = \frac{I_n - C_r\left(V_{\mathrm{Load}_{n-1}} + V_{d2}\right)\lambda_2}{C_r(\lambda_1 - \lambda_2)};$$
$$B_n = \frac{C_r\left(V_{\mathrm{Load}_{n-1}} + V_{d2}\right)\lambda_1 - I_n}{C_r(\lambda_1 - \lambda_2)}. \tag{12}$$

3.3. Energy discharging loop

By observing equations (11) and (12), it is found that the synchronous current I_{sec} in the n^{th} EC phase is still not determined due to the unknown values of $V_{\mathrm{Load}_{n-1}}$. A simple method is to assume a constant value for the load voltage. However, the storage capacitor C_r is charged by the EC loop and discharged by the ED loop. That means the load voltage is always changing between the synchronous instants. Consequently, assuming a constant V_{Load} will affect the accuracy of the energy flow analysis, and thus, the determination of the optimal VFSs.

In this regard, the discharging loop is especially considered at this stage to obtain the exact dynamic load voltages. As shown in figure 1(b), EC happens at synchronous instants with a relatively short period, while energy discharging lasts during half of the mechanical period $T_{\mathrm{ME}}/2$. In the case of stable equilibrium, V_{Load} would be stable, following the repetitive curves ($V_{\mathrm{Load}_0} \to V_{\mathrm{Load}_1} \to V_{\mathrm{Load}_2} \to V_{\mathrm{Load}_3} \to V_{\mathrm{Load}_0}$) as seen in figure 1(d). Consequently, the relationships between the initial load voltage V_{Load_0} and the last load voltage V_{Load_N} can be established in both ED and EC loops,

$$V_{\mathrm{Load}_0} = V_{\mathrm{Load}_N} e^{-\frac{T_{\mathrm{ME}}/2}{R_L C_r}} = V_{\mathrm{Load}_N} e^{-\frac{\pi}{R_L C_r \omega}}. \tag{13}$$

The first relationship is described as equation (13), which is based on the RC transient response of the ED loop during a period of $T_{\mathrm{ME}}/2$. In the EC loops, the relationship between V_{Load_0} and V_{Load_n} ($n = 1, \ldots, N$) can be expressed step-by-step. Firstly, the time period t_{sec_n} is solved by using equation (11) with the boundary conditions of I_n and the initial load voltage $V_{\mathrm{Load}_{n-1}}$ for the n^{th} EC phase. Then, the expression of t_{sec_n} is substituted into equation (10) to derive the expression of load voltage V_{Load_n}, which is then used as the initial load voltage for the next EC step. By repeating this process, all expressions of V_{Load_n} and t_{sec_n} with respect to V_{Load_0} can be derived. A more detailed calculation process is presented in figure 3. Consequently, the values of V_{Load_0} and V_{Load_N} can be simultaneously solved by the two corresponding relationships in the EC and ED loops, allowing the values of V_{Load_n} and t_{sec_n} to be numerically obtained as well. Then, the dissipations caused in the n^{th} EC phase and the corresponding energy flow relationship can be expressed as

$$E_{d\_\mathrm{sec}_n} = E_{d\_\mathrm{sec}\_r_n} + E_{d\_\mathrm{sec}\_d_n} = \int_0^{t_{\mathrm{sec}_n}} I_{\mathrm{sec}}^2 r_2 \mathrm{d}t + \int_0^{t_{\mathrm{sec}_n}} V_{d2} I_{\mathrm{sec}} \mathrm{d}t \tag{14}$$

$$E_{\mathrm{sto}_n} = \frac{1}{2}C_r\left(V_{\mathrm{load}_n}^2 - V_{\mathrm{load}_{n-1}}^2\right) = E_{L_n} - E_{d\_\mathrm{sec}_n} \tag{15}$$

where $E_{d\_\mathrm{sec}_n}$ and E_{sto_n} represent the dissipation energy and the harvested energy in the n^{th} EC phase.

3.4. Electrical efficiency

The energy flows (E_{ext}, E_{sto}, E_{d_pri}, E_{d_sec}) in the SECE circuit are the sums of their counterparts in each single step. Then, the electrical efficiencies can be defined as

$$\eta_{\mathrm{ET}} = \frac{E_L}{E_{\mathrm{ext}}}, \eta_{\mathrm{EC}} = \frac{E_{\mathrm{sto}}}{E_L}, \eta_{\mathrm{elec}} = \frac{E_{\mathrm{sto}}}{E_{\mathrm{ext}}}, \eta_{\mathrm{elec}} = \eta_{\mathrm{ET}} \times \eta_{\mathrm{EC}} \tag{16}$$

where, η_{ET} is the electrical efficiency of the ET phase, η_{EC} is the electrical efficiency of the EC phase, and η_{elec} is the overall electrical efficiency. The electrical efficiencies vary under different VFSs, and the optimal VFSs will result in a maximum η_{elec}.

Clearly, the established theoretical model can evaluate the electrical efficiencies for the SECE circuit with different VFSs. Some advantages and advancements can be inferred:

(1) The resistive dissipation of the ET phase is calculated more accurately by the behavior of synchronous current in the ET phase over specific time periods. It is a big step forward than the conventional approach, which relies on rough estimation by the inversion factor γ [30];
(2) Both resistive and diode dissipations can be accurately evaluated by numerically solving for the load voltage and the behavior of the secondary synchronous current. Therefore, the dissipations in the EC phase, which are

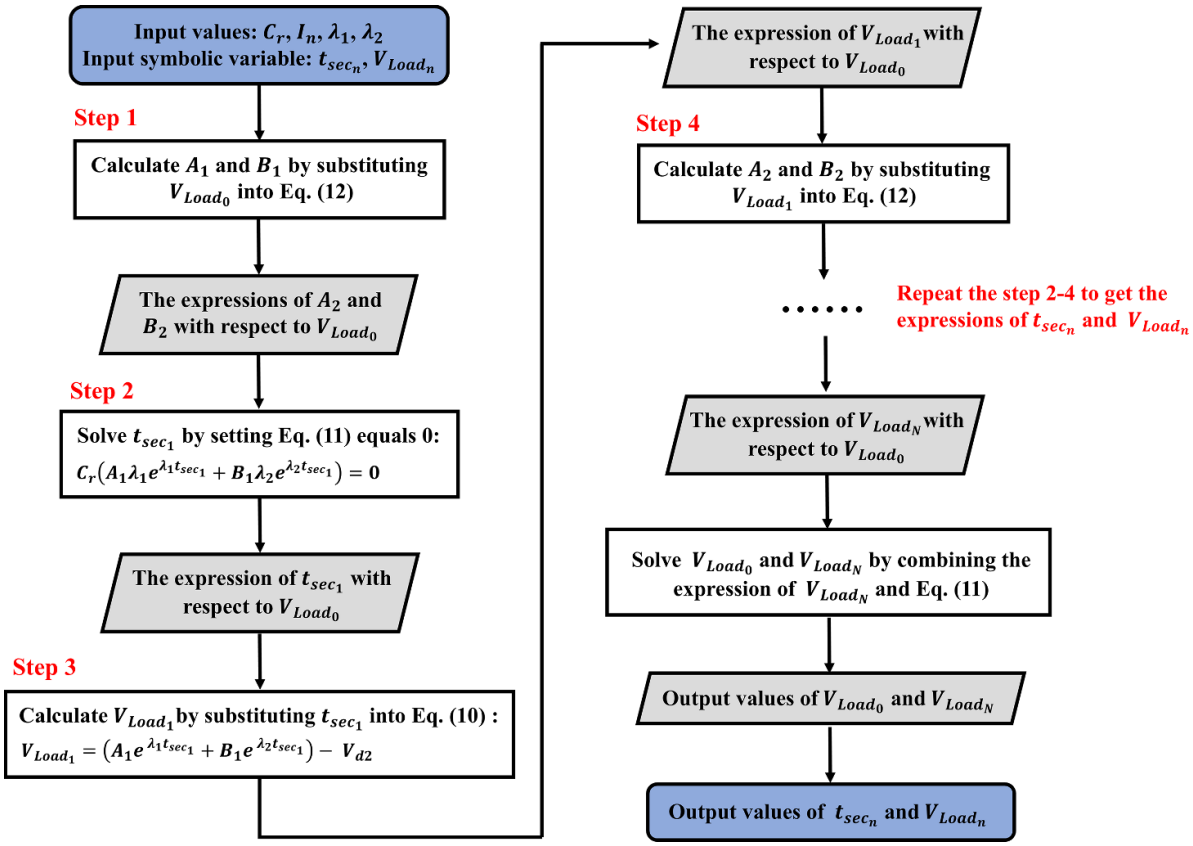

Figure 3. The flow chart of solving the values of load voltages and time periods for the EC phases.

often neglected or less considered, can be precisely evaluated as well;

(3) The proposed model enables the analysis of the overall electrical efficiency with different VFSs and helps identify the optimal VFSs.

To verify the accuracy of the proposed model, the proportions of energy flows within the SECE circuit and a 3S-SECE are presented in figure 4. The simulated parameters are presented in table 1. For the SECE circuit, the harvested and dissipation energies in the ET and EC phases of the SECE circuit as a fraction of one are shown in figure 4(a). The sum of three components always equals 1, indicating that the proposed model can precisely describe every energy flow out of the extracted energy E_{ext}. Obviously, the conventional models in [30] and [31] tend to overestimate the harvested energy due to the insufficient consideration of various types of dissipation energies. Notably, the dissipation energies in the EC phase E_{d_sec}, usually partly considered or neglected in previous studies, is close to 0.1, which appears to be important enough for evaluating the electrical efficiency of the SECE circuit. Figure 4(c) displays the four components of the dissipation energies caused by r_1, D_1, r_2 and D_2, respectively. As a reference, the resistive dissipation $E_{d\_\text{pri}\_r}$ predicted by the inversion factor γ is indicated by the black dotted line, which is obviously lower than that predicted by the proposed model. In addition, the dissipation energies in the EC phase are precisely described as well. Particularly, resistive dissipation $E_{d\_\text{sec}\_r}$ may account for a large proportion when V_{p_0} is relatively large, however, it has seldom been given attention in previous studies.

Figures 4(b) and (d) show the proportions of energy flows within a 3S-SECE circuit. The VFS is set to $V_{p_0} = 20\text{V} \rightarrow 0.6V_{p_0} \rightarrow 0.4V_{p_0} \rightarrow 0$. Figure 4(b) reveals that the improvement of the harvested energy E_{sto} mainly benefits from the reduced resistive dissipation $E_{d\_\text{pri}\_r}$ in the ET phase, while both dissipation energies $E_{d\_\text{sec}\_r}$ and $E_{d\_\text{sec}\_d}$ in the EC phases nearly retain constant. Furthermore, the amount of the diode dissipation $E_{d\_\text{pri}\_d}$ for the ET phases remains unchanged as depicted in figures 4(c) and (d), as it is only determined by the initial voltage V_{p_0} according to equation (17),

$$E_{d\_\text{pri}\_d} = \sum_{1}^{n} \int_{0}^{t_{\text{pri}_n}} V_{d1} I_{\text{pri}} dt = C_p V_{p_0} V_{d1}. \tag{17}$$

From the above analysis, it is evident that the proposed model significantly improves the accuracy in comparison with previous ones. It reveals that the diode D_2 and the resistance r_2 takes a non-negligible part of the total energy at the synchronous instants with a relatively fixed value, which will become more significant for the MS-SECE circuit as the overall electrical efficiency is increased in this case.

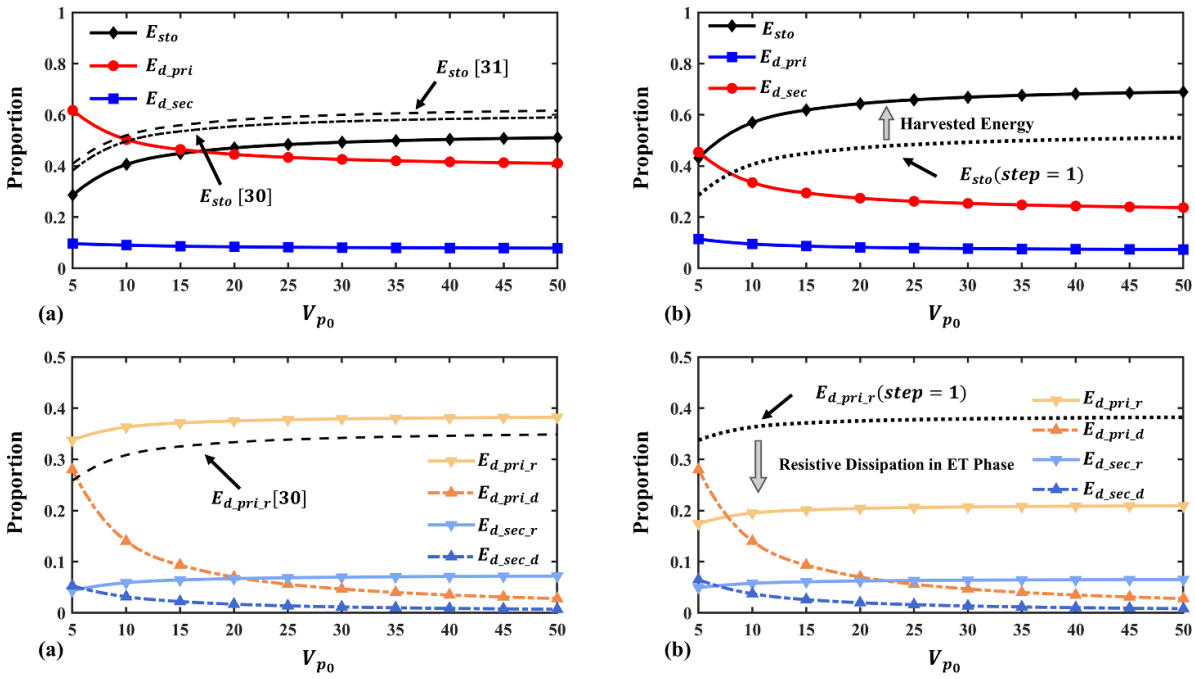

Figure 4. Proportions of energy flows in the SECE circuit. (a) Energy flow proportion for the standard SECE circuit; (b) energy flow proportion for a 3S-SECE circuit; (c) dissipation proportion for the standard SECE circuit. (d) Dissipation proportion for a 3S-SECE circuit.

4. Optimization of MSEE strategy

With the proposed model, the optimal VFSs can be derived by evaluating the electrical efficiencies of the MS-SECE circuit. To simplify the expression, the normalized intermediate voltage $\tilde{V}_n$ is defined as

$$\tilde{V}_n = \frac{V_{p_n}}{V_{p_0}}. \tag{18}$$

By this way, the VFSs can be denoted as a sequence of numbers between 1 and 0. For instance, the VFS of $V_{p_0} \rightarrow V_{p_1} = 0.8V_{p_0} \rightarrow V_{p_2} = 0.4V_{p_0} \rightarrow V_{p_3} = 0$ can be expressed as the normalized form of $\tilde{V}_0 = 1 \rightarrow \tilde{V}_1 = 0.8 \rightarrow \tilde{V}_2 = 0.4 \rightarrow \tilde{V}_3 = 0$. The simulation parameters used in this section are presented in table 1.

Table 1. Simulation parameters of the SECE circuit.

Variable	Quantity	Value
C_p	Piezoelectric capacitance	200 nF
L	Inductance	1 mH
V_{d1}&V_{d2}	Diode voltage drops in ET and EC loops	0.7 V
r_1&r_2	Parasitic resistances in ET and EC loops	20 Ω
Q_I	Quality factor of ET loop	3.54
C_{sto}	Storage capacitance	470 μF
R_L	Load resistance	200 kΩ
T_{ME}	Mechanical vibration period	0.02 s

4.1. Optimal VFSs for 2S-SECE and 3S-SECE circuits

For the 2S-SECE circuit, the piezoelectric voltage would undergo $V_{p_0} \rightarrow V_{p_1} \rightarrow 0$, which means that only the intermediate voltage $\tilde{V}_1$ needs to be determined for a specific V_{p_0}. Figure 5 shows the simulated results of the electrical efficiencies η_{ET}, η_{EC}, η_{elec} with respect to $\tilde{V}_1$ and V_{p_0}. The blue line in figure 5(a) clearly depicts that η_{ET} first increases and then decreases as $\tilde{V}_1$ increases. The maximum value of η_{ET} occurring at $\tilde{V}_1 = 0.55$, which is independent of V_{p_0} as the red line highlights. By contrast, the electrical efficiency of the EC phase η_{EC} is almost unaffected by $\tilde{V}_1$ as the blue line highlights, varying in a small range from around 0.8–0.9 as shown in figure 5(b). Then, the overall electrical efficiency η_{elec} is calculated by the product of η_{ET} and η_{CT}, and its variation trend is similar to that of η_{ET} as depicted in figure 5(c). As the red line highlights, the location of the optimal $\tilde{V}_1$ for η_{elec} slightly shifts to 0.6 although the optimal $\tilde{V}_1$ for η_{EC} occurs at 0.775. It indicates the optimal VFS for η_{elec} is little influenced by η_{CE}. More significantly, it remains independent of V_{p_0}. Therefore, the optimal VFS for the 2S-SECE circuit is initially determined as 1–0.6–0.

Next, the electrical efficiencies of the 3S-SECE circuit are analyzed to determine the optimal $\tilde{V}_1$ and $\tilde{V}_2$. Figure 6 shows the electrical efficiencies η_{ET}, η_{EC} and η_{elec} under different VFSs at $V_{p_0} = 20$ V, in which both two-step (2S) and three-step (3S) cases are presented. The left side area of the blue lines $\left(\tilde{V}_1 \leqslant \tilde{V}_2\right)$ represents the 2S-SECE circuit where $\tilde{V}_2$ is set equal to $\tilde{V}_1$ to eliminate the second step, and thus, the electrical efficiencies are only influenced by $\tilde{V}_1$. The right-side area $\left(\tilde{V}_1 > \tilde{V}_2\right)$ refers to the 3S case where the values of η_{ET}

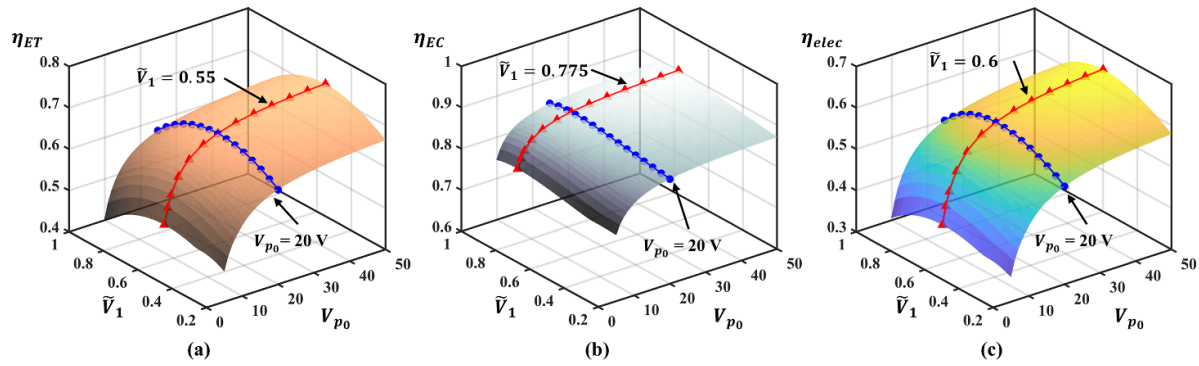

Figure 5. The electrical efficiencies of the 2S-SECE circuit. (a) Electrical efficiency of the ET phases; (b) electrical efficiency of the EC phases; (c) overall electrical efficiency.

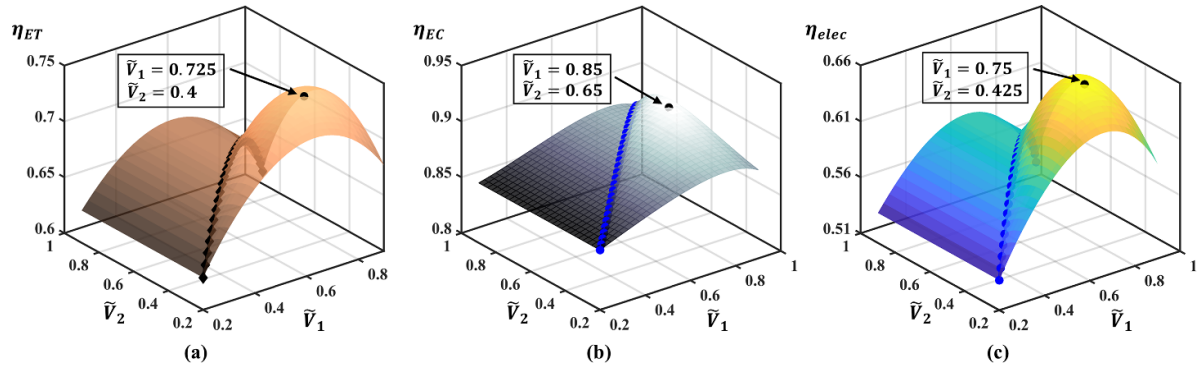

Figure 6. The electrical efficiencies of the 3S-SECE circuit. (a) Electrical efficiency of the ET phases; (b) electrical efficiency of the EC phases; (c) overall electrical efficiency.

and η_{elec} in figures 6(a) and (c) are always larger than those in the 2S area, indicating that an additional step can further enhance the electrical efficiency on the basis of the 2S-SECE circuit. Meanwhile, η_{EC} still fluctuates within a relatively small range as shown in figure 6(b) with the optimal VFS for η_{EC} identified as 1–0.85–0.65–0. As a result, the overall electrical efficiency η_{elec} is still dominated by the ET phase in this case. Considering the controllability in practice, the optimal VFS for the 3S-SECE circuit is initially determined as 1–0.7–0.4–0.

Based on the above analysis, we can primarily conclude that the MSEE strategy enhances η_{elec} of the SECE circuit mainly by improving η_{ET}, but less η_{EC}. In other words, η_{EC} has minimal influence on the optimal VFS for η_{elec}. In fact, the value of η_{EC} is evaluated under the steady state for the SECE circuit when the charged and discharged energy in EC and ED loops are exactly the same during half of the mechanical period. However, the steady-state is hardly achieved in practice since the storage capacitor needs to be connected to a DC–DC converter, such as LTC3588 [33], instead of a pure resistor. In these scenarios, the load condition of the SECE circuit varies most of the time. Therefore, it is hard to precisely estimate η_{EC} under a dynamic occasion. Generally, a larger storage capacitor is used to harvest more energy, thereby minimizing the influence of η_{EC} on η_{elec} and optimal VFSs owing to a more stable V_{Load}.

Thanks to the little influence of the EC phases, it is reasonable to focus on η_{ET} as the primary object to optimize the MSEE strategy. To get a general result of the optimal VFSs for the MS-SECE circuits under different intrinsic parameters, such as r_1, C_p and L, the influence of the diode dissipation in the ET phase $E_{d\_\text{pri}\_d}$ should be eliminated since it only introduces a bias effect on η_{ET} [34]. Therefore, the bias intermediate voltage V'_{p_n} and normalized bias intermediate voltage $\tilde{V}'_n$ are defined in equation (19). Then, the electrical improvement of the ET phases$\eta_{\text{Imp_ET}}$ is defined as equation (20) to reflect the effectiveness of the MSEE strategy,

$$V'_{p_n} = V_{p_n} - V_{d1}, \tilde{V}'_n = \frac{V'_{p_n}}{V'_{p_0}}. \tag{19}$$

$$\eta_{\text{Imp\_ET}} = \frac{E_{L(\text{MS}-\text{SECE})}}{E_{L(\text{SECE})}}. \tag{20}$$

Substituting equation (19) into equation (5) and combining it with equation (20) will lead to the expression of the electrical improvement of the ET phases as

$$\eta_{\text{Imp\_ET}} = \frac{\sum_1^N \left(\tilde{V}'^2_{n-1} \sin^2 \left(\omega_{LC} \sqrt{1-(1/2Q_I)^2}\, t_{\text{pri}_n} \right) \mathrm{e}^{-\frac{\omega_{LC}}{Q_I} t_{\text{pri}_n}} \right)}{\sin^2 \left(\omega_{LC} \sqrt{1-(1/2Q_I)^2}\, t_{\text{pri}_0} \right) \mathrm{e}^{-\frac{\omega_{LC}}{Q_I} t_{\text{pri}_0}}} \tag{21}$$

where N is the total step number of the MSEE strategy, t_{pri_0} is the time period of the ET phase for the SECE circuit, and t_{pri_n}

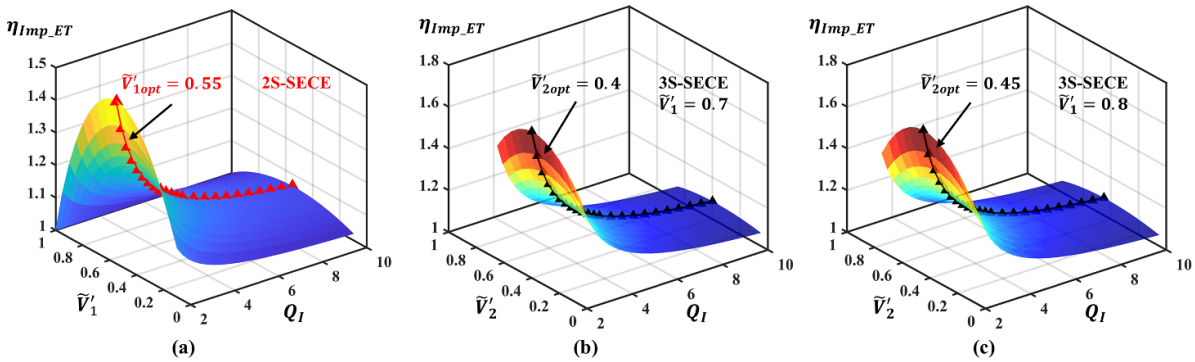

Figure 7. Electrical improvement of the ET phases with respect to the circuit quality factor and the normalized bias intermediate voltage. (a) 2S-SECE circuit; (b) 3S-SECE circuit, $\tilde{V}'_1 = 0.7$; (b) 3S-SECE circuit, $\tilde{V}'_1 = 0.8$.

are those for the MS-SECE circuit. The values of t_{pri_0} and t_{pri_n} can be numerically calculated according to equation (4) once the sequence of $\tilde{V}'_n$ is decided.

Since V_{p_0} is always much larger than V_{d1} in practice, it is reasonable to take the optimal VFSs of $\tilde{V}'_n$ as those of $\tilde{V}_n$ most of the time by assuming $\tilde{V}'_n \approx \tilde{V}_n$. Moreover, the bias effect of the diode can be further eliminated by adopting a rectifier-less topology [35–37]. By defining V'_{p_n} and $\tilde{V}'_n$, the expression of $\eta_{\text{Imp\_ET}}$ is simplified, which only depends on the circuit quality factor Q_I and the natural angular frequency ω_{LC} of the ET loop as described by equation (21). Further investigation of equation (21) reveals that $\eta_{\text{Imp\_ET}}$ is independent of ω_{LC} since only Q_I relates to r_1 as defined in equation (6). Besides, the enhancement of $\eta_{\text{Imp\_ET}}$ purely attributes to the reduction of the resistive dissipation $E_{d\_\text{pri}\_r}$ as the bias effect of the diode has been eliminated. Therefore, Q_I will be the exclusive criteria for evaluating $\eta_{\text{Imp\_ET}}$ in the following analysis.

Figure 7(a) shows the electrical improvement of the ET phases $\eta_{\text{Imp\_ET}}$ for the 2S-SECE circuit with respect to Q_I and $\tilde{V}'_1$. It is observed that $\eta_{\text{Imp\_ET}}$ significantly increases when Q_I is relatively smaller, suggesting that the MSEE strategy becomes more effective in the lower electrical efficiency cases. Noticeably, the optimal cases are achieved when $\tilde{V}'_{1\text{opt}}$ is 0.55, regardless of the value of Q_I. It indicates that 0.55 could be considered the optimal $\tilde{V}'_{1\text{opt}}$ for the 2S-SECE circuit across different intrinsic parameters since Q_I is defined by r_1, C_p, and L simultaneously. Combining with the results from figure 5(c), the above proposed VFS 1–0.6–0 can be regarded as the general optimal VFS in consideration of η_{elec}.

Similarly, figures 7(b) and (c) display $\eta_{\text{Imp\_ET}}$ for the 3 S-SECE circuit with respect to Q_I and $\tilde{V}'_2$. The studied values of $\tilde{V}'_1$ are selected as 0.7 and 0.8 based on the primary results from figure 6. It is evident that $\eta_{\text{Imp\_ET}}$ first increases and then decreases as $\tilde{V}'_2$ increases, and the optimal $\tilde{V}'_{2opt}$ are 0.4 and 0.45, respectively. The values correspond to the value of $\tilde{V}'_{1\text{opt}}$ for the 2S-SECE circuit for a specific $\tilde{V}'_1$. For instance, $0.45/0.8 \approx 0.55$. More importantly, the values of $\tilde{V}'_2$ remains independent of Q_I. These findings indicate that the 3-step case can be regarded as the sum of a 2-step and a single-step case, providing a foundation for deriving the optimal VFSs for the MS-SECE circuit in the following analysis. Additionally, the optimal values of $\eta_{\text{Imp\_ET}}$ for the two selected $\tilde{V}'_1$ are relatively close, which is advantageous in practice since the switching time cannot be precisely controlled to achieve a concrete optimal VFS. Moreover, the influence of the EC phase can be further reduced when the optimal VFS is defined in a small region. Consequently, the optimal VFS can be achieved around 1–0.7–0.4–0.

4.2. Optimal VFSs for MS-SECE circuits

To further explore the potential of the MSEE strategy, the optimal VFSs for the MS-SECE circuit are analyzed by using a recursive method. For the feasibility, the method is carried out based on the electrical improvement of the ET phases $\eta_{\text{Imp\_ET}}$. The core concept is to take an N-step MS-SECE circuit as a 2S case, where the first step contains a single step and the second step contains N-1 sub-steps. Therefore, $\eta_{\text{Imp\_ET}}$ can be revised as

$$\eta_{\text{Imp\_ET}} = \frac{E_{L_1} + E_{L_{(2-N)}}}{E_{L(\text{SECE})}} \quad . \tag{22}$$

In equation (22), E_{L_1} is the inductive energy transferred by the first (single) step, $E_{L_{(2-N)}}$ refers to the total inductive energy for the subsequent N-1 steps. Once the first normalized bias intermediate voltage $\tilde{V}'_1$ is determined, E_{L_1} can be calculated. Then, the second step can be directly optimized, as the maximum inductive energy $E_{L_{(2-N)}}$ will occur under the optimal VFS for the (N-1)-step case. For instance, given that the optimal $\tilde{V}'_1$ for the 2S-SECE circuit is 0.55, the optimal $\tilde{V}'_2$ for the 3S-SECE circuit will be directly obtained as $0.55^* \tilde{V}'_1$ for a specific $\tilde{V}'_1$. The recursive method allows for determining the optimal VFSs for the N-step MS-SECE circuit by analyzing $\tilde{V}'_1$ instead of all $\tilde{V}'_n$. Thus, the N-variable question is reduced to a two-variable one.

Figure 8(a) shows $\eta_{\text{Imp\_ET}}$ for the MS-SECE circuit with respect to $\tilde{V}'_1$. To start with, $\eta_{\text{Imp\_ET}}$ for the 2S-SECE circuit is directly calculated by equation (21) as presented by the purple line in figure 8(a). The optimal $\tilde{V}'_{1\text{opt}\_2S}$ occurs at 0.55, referring to the optimal VFS as 1–0.55–0. Subsequently, $\eta_{\text{Imp\_ET}}$ for the 3S-SECE circuit is calculated under different values of $\tilde{V}'_1$ with the corresponding optimal $\tilde{V}'_2$ identified as $0.55^* \tilde{V}'_1$. In this case, $\tilde{V}'_{1\text{opt}\_3S}$ is obtained as 0.725, and thus the corresponding $\tilde{V}'_{2\text{opt}\_3S}$ is calculated as $\tilde{V}'_{1\text{opt}\_2S} * \tilde{V}'_{1\text{opt}\_3S} \approx 0.4$. Therefore, the

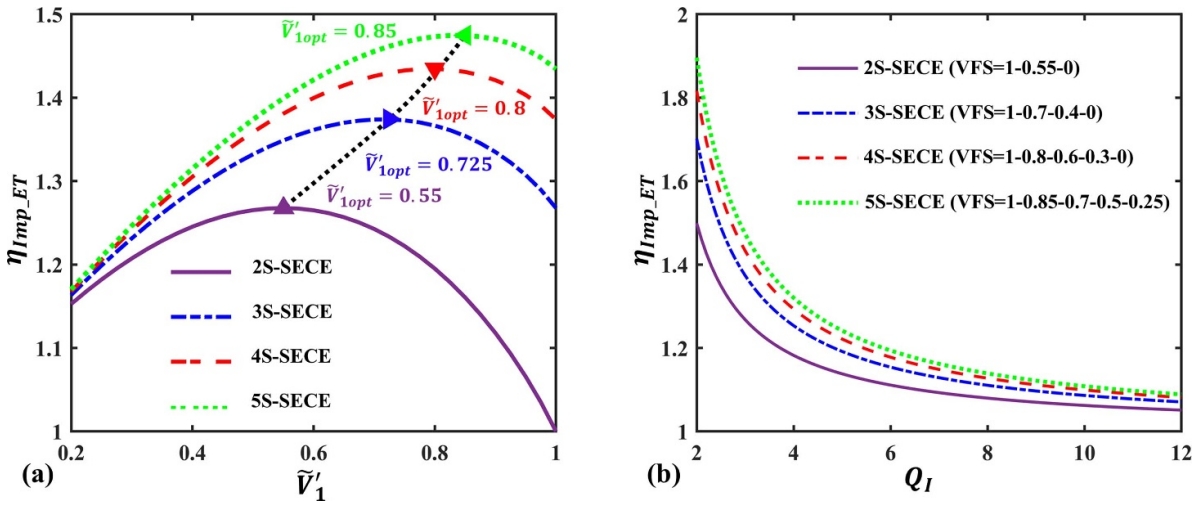

Figure 8. Electrical improvement of the ET phases for the MS-SECE circuits. (a) Electrical improvement of the ET phases with respect to the first normalized bias intermediate voltage; (b) Electrical improvement of the ET phases under the proposed optimal VFSs.

Table 2. Summarized optimal VFSs for the MS-SECE circuit.

Number of Steps	Optimal VFS	Number of Steps	Optimal VFS
2	1–0.6–0	4	1–0.8–0.6–0.3–0
3	1–0.7–0.4–0	5	1–0.85–0.7–0.5–0.25–0

recursively obtained optimal VFS for the 3S-SECE circuit as 1–0.725–0.4–0. By repeating the above processes, $\eta_{\mathrm{Imp\_ET}}$ and $\tilde{V}'_{\mathrm{1opt}}$ for the MS-SECE circuits can be obtained step-by-step. Finally, $\tilde{V}'_{\mathrm{1opt\_4S}}$ and $\tilde{V}'_{\mathrm{1opt\_5S}}$ are obtained as 0.8 and 0.85, with the optimal VFSs calculated as 1–0.8–0.58–0.3–0 and 1–0.85–0.68–0.49–0.27–0, respectively

Once again, it should be noted that the electrical efficiency of the EC phase is variable in practice but always has minimal influence on the locations of the optimal VFSs. The proposed optimal VFSs can be simply converted into the switching time series and implemented. Considering the controllability, the recommended optimal VFSs for the N-step (N = 2–5) MS-SECE circuits are summarized in table 2 based on the conclusions in this section, which can be referred to optimize the performance of the MS-SECE circuit. Figure 8(b) shows the electrical improvement $\eta_{\mathrm{Imp\_ET}}$ under the optimal VFSs in table 2. Notably, considering that the incremental benefit of an additional step becomes less significant for N $\geqslant$ 3, it is advisable to use N = 3 for straightforward implementation for most cases. The 2S-SECE circuit may be more suitable for small voltage cases since the third step would only bring insignificant additional harvested power. Under larger voltage cases, the adopted number of steps can be larger for further enhanced performance. However, the harvested power may not increase all the time with more steps in practice since the parasitic loss of the diode transistors might increase with more synchronous actions triggered.

5. Experiment

5.1. Setup

A piezoelectric cantilever harvester with an SECE circuit is fabricated for the test. The excitation frequency was set as 35.5 Hz in the experiments, and the piezoelectric capacitor was measured as 208 nF. The other selected parameters in the circuit are the same as those listed in table 1. The established experimental platform is shown in figure 9. The harvester is placed on the shaker (The Modal Shop©, 2075E-HT). A signal generator (RIGOL©, DG2052) is used to excite the shaker through a power amplifier. An MCU (STM32L431) is used to generate the switch control signals. The current waveform during the LC oscillation is detected by a current probe (Tektronix©, TCPA300), the load voltage is measured by a digital multimeter (RIGOL©, DM3085E), while the oscilloscope (Tektronix©, MDO3024) is used to capture voltage and current waveforms. Two experimental cases were carried out. The first case under a constant initial voltage ($V_{p_0} = 20$ V) is used to validate the optimal VFSs for the 2S-SECE and 3S-SECE circuits and the accuracy of the proposed theoretical model. The second case is used to investigate the effectiveness of the MSEE strategy on the SECE circuit.

Figure 10 shows the experimental waveforms of different MS-SECE circuits. The overall view of the piezoelectric voltage waveforms is the same, which suggests that the MSEE strategy does not influence the dynamics of the

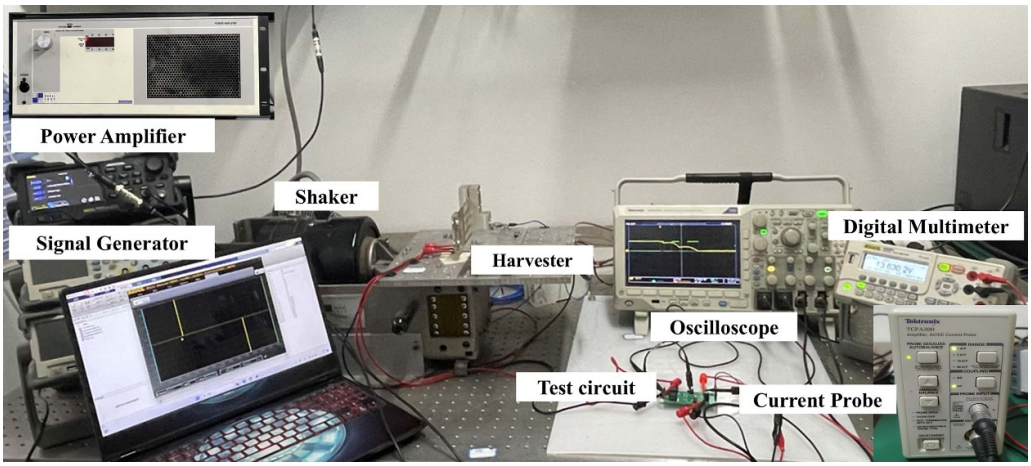

Figure 9. The experimental platform for the MS-SECE circuit.

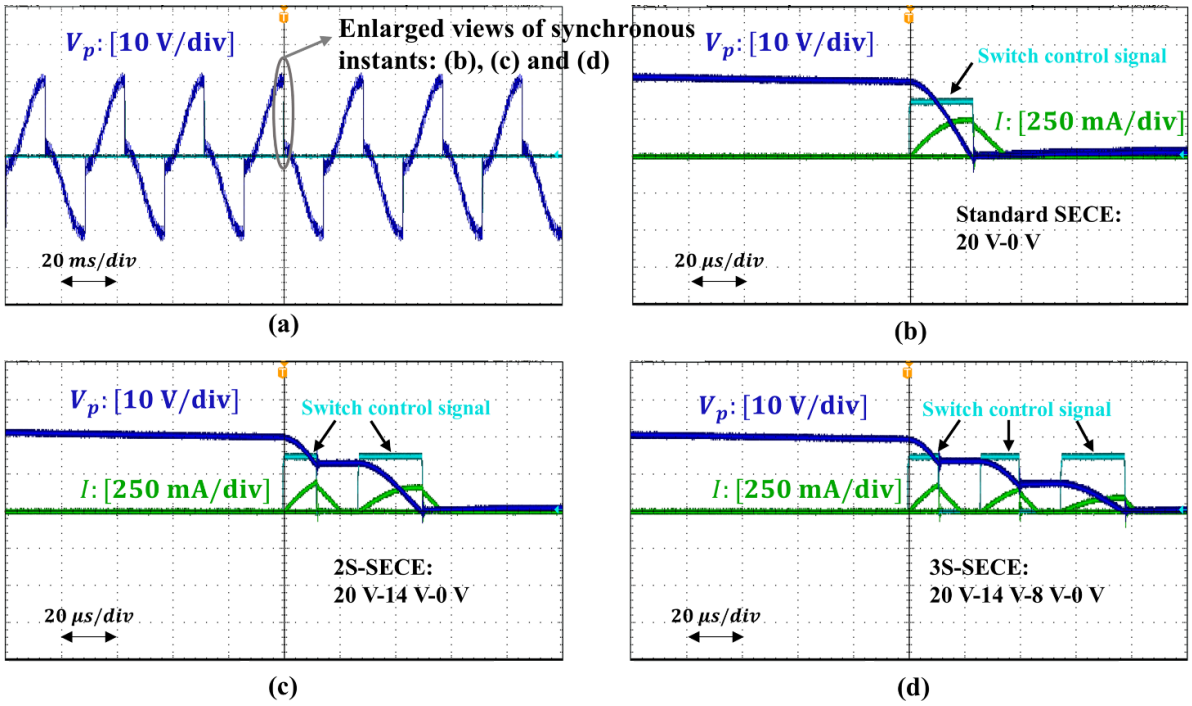

Figure 10. Experimental waveforms of the MS-SECE circuit. (a) The overall view of piezoelectric voltage; (b), (c) and (d) the enlarged views of the synchronous instants for the SECE, 2S-SECE and 3S-SECE circuits, respectively.

electromechanical system. The enlarged views, figures 10(b)–(d), display the detailed waveforms at the synchronous instants for the SECE, 2S-SECE and 3S-SECE circuits. The electrical efficiency is calculated as the ratio of the harvested energy to the extracted energy within a single mechanical period T_{ME}. Once the conditions (VFS or V_{p_0}) are changed, the load voltage will increase or decrease to a new steady state. Then, the electrical efficiency is calculated by the V_{p_0} and V_{load} according to equation (23),

$$\eta_{\mathrm{elec\_exp}} = \frac{C_p V_{p_0}^2}{V_{\mathrm{load}}^2 * \frac{T_{\mathrm{ME}}}{R_L}} \tag{23}$$

5.2. Results

With an initial voltage of 20 V, figure 11(a) compares the theoretical and experimental results of the overall electrical efficiency η_{elec} of the 2S-SECE circuit with respect to the first intermediate voltage $\tilde{V}_1$. η_{elec} initially increases and then decreases as $\tilde{V}_1$ increases with the maximum value of η_{elec} occurring at $\tilde{V}_1 = 0.6$. The experimental results show good agreement with the theoretical one when the values of parasitic resistances r_1 and r_2 are identified to be 16 Ω. The experimental results of the 3S-SECE circuit at $\tilde{V}_1 = 0.6$, 0.7 and 0.8 are presented in figure 11(b). It is obvious to find that the trend of η_{elec} is similar to that of the 2S case once $\tilde{V}_1$ is determined.

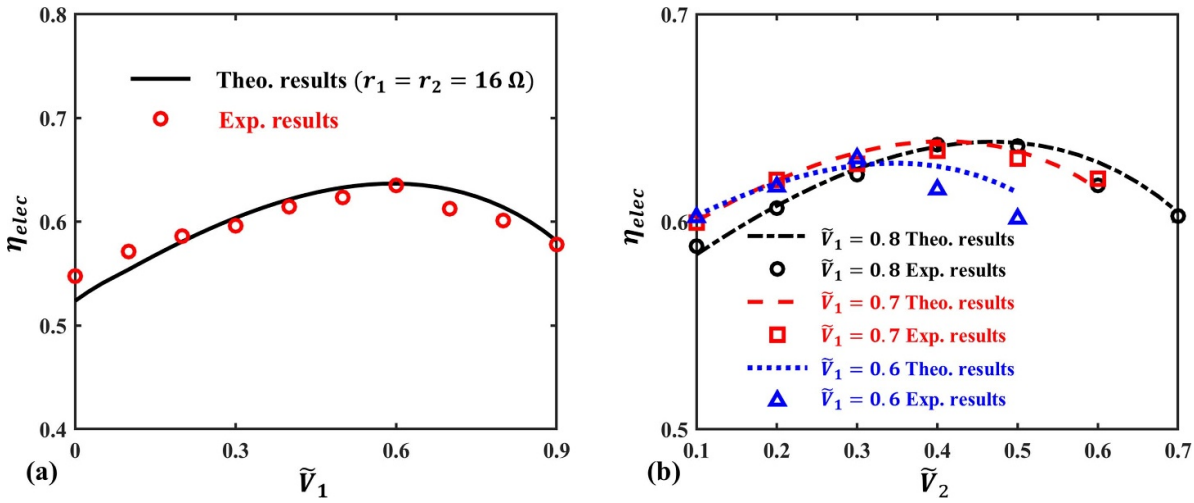

Figure 11. Overall electrical efficiency of the 2S-SECE and 3S-SECE circuits under different VFSs. (a) 2S-SECE circuit; (b) 3S-SECE circuit.

The local extremes of η_{elec} can be easily obtained for each $\tilde{V}_1$ case with the corresponding VFSs located around 1–0.8–0.5–0, 1–0.7–0.4–0 and 1–0.6–0.3–0. Notably, the first two VFSs provide similar and outperformed results, which are consistent with the theoretical results. In this case, the identified parasitic resistances are revised to be 20 Ω, which suggests that the values of parasitic effects may exhibit a nonlinear characteristic for the MS-SECE circuit with different steps. The phenomenon may be attributed to the fact that more synchronous actions are triggered at the instant, resulting in a greater parasitic loss caused by the diode and switching MOSFET in the circuit [34, 38]. It also hinted that the effectiveness of the MSEE strategy in real applications may not increase all the time with more steps. Despite this, the proposed theoretical mode remains meaningful since the primary aim is to propose the general optimal VFSs for the MS-SECE circuit, and they have been proven to be unaffected by the values of parasitic resistances or quality factor in theory. Moreover, good accordance between experiments and theory is still observed.

In order to verify the effectiveness of the MSEE strategy in real applications, the electrical efficiency and the electrical improvement were measured by using two PCB circuits with different circuit quality factors, $Q_{I\_\text{low}} \approx 3.5$ and $Q_{I\_\text{high}} \approx 4.6$, respectively. Figures 12(a) and (b) show the overall electrical efficiency η_{elec} of the SECE, 2S-SECE and 3S-SECE circuits under the optimal VFSs summarized in table 2. As the initial voltage V_{p_0} increases, η_{elec} sharply increases at first, then gradually stabilizes. This phenomenon is caused by the constant diode dissipation energies, which take a significant part of the total energy when V_{p_0} is relatively small, and their proportions decrease rapidly under larger V_{p_0}. A slight decrease of η_{elec} is observed when V_{p_0} is larger, which can be attributed to the dielectric loss in piezoelectric element [39] or nonlinear parasitic effects in electronic elements. With the optimal VFSs applied, similar performance is obtained for the two circuits with different Q_I, suggesting that the MSEE strategy can equivalently enhance the circuit quality factor of the SECE circuit, which is a critical factor for improving the performance of synchronous switching circuits.

The enhanced ratio of the overall electrical efficiency $\eta_{\text{Enh\_elec}}$ of the 2S-SECE and 3S-SECE circuits are presented in figures 12(c) and (d). Obviously, $\eta_{\text{Enh\_elec}}$ gradually declines with the increase of V_{p_0}, which is attributed to the bias effect of the diode dissipations. Moreover, larger $\eta_{\text{Enh\_elec}}$ is observed for the lower Q_I circuit with the corresponding values for the 2S and 3S cases measured as 41.9% and 65.5% under an extremely low initial voltage ($V_{p_0} = 2.5$ V), and 5.8%, 9.4% under a large initial voltage ($V_{p_0} = 40$ V). By contrast, the values for the higher Q_I circuit were 20.8%, 38.3% and 4.1%, 7.2%, respectively.

In summary, the experimental results verified the effectiveness of the MSEE strategy on the SECE circuit, and proved the accuracy of the proposed model and the proposed optimal VFSs. It also indicates that the MSEE strategy is more effective under lower circuit quality factor. Furthermore, the proposed optimal VFSs can be used as a reference for the MS-SECE circuits to achieve a better performance.

5.3. Discussion

The implementation of the MSEE strategy generally requires an additional controller to generate the PWM waves to execute the MS switching actions. The proposed optimal VFSs can be easily converted into the corresponding PWM waves or switching time according to the intrinsic parameters of the electromechanical system. During the experiment, the switching time was set to 12 us, 21 μs, and 10 us, 13 us, 21 us to carry out the optimal VFSs 1–0.6–0 and 1–0.7–0.4–0 for the 2S-SECE and 3S-SECE circuits, respectively. Figure 13(a) displays the harvested power of the SECE, 2S-SECE, and 3S-SECE circuits of the lower Q_I circuit, while figure 13(b) shows the additional harvested power for the 2S-SECE and 3S-SECE circuits on the basis of the SECE circuit. It is evident that a larger power difference is observed with a higher initial voltage V_{p_0} despite less electrical improvement in these cases. Moreover, the additional harvested power between the 3-step and 2-step cases is enlarged as well. Specifically, at a typical initial voltage of 20 V, the power differences for the

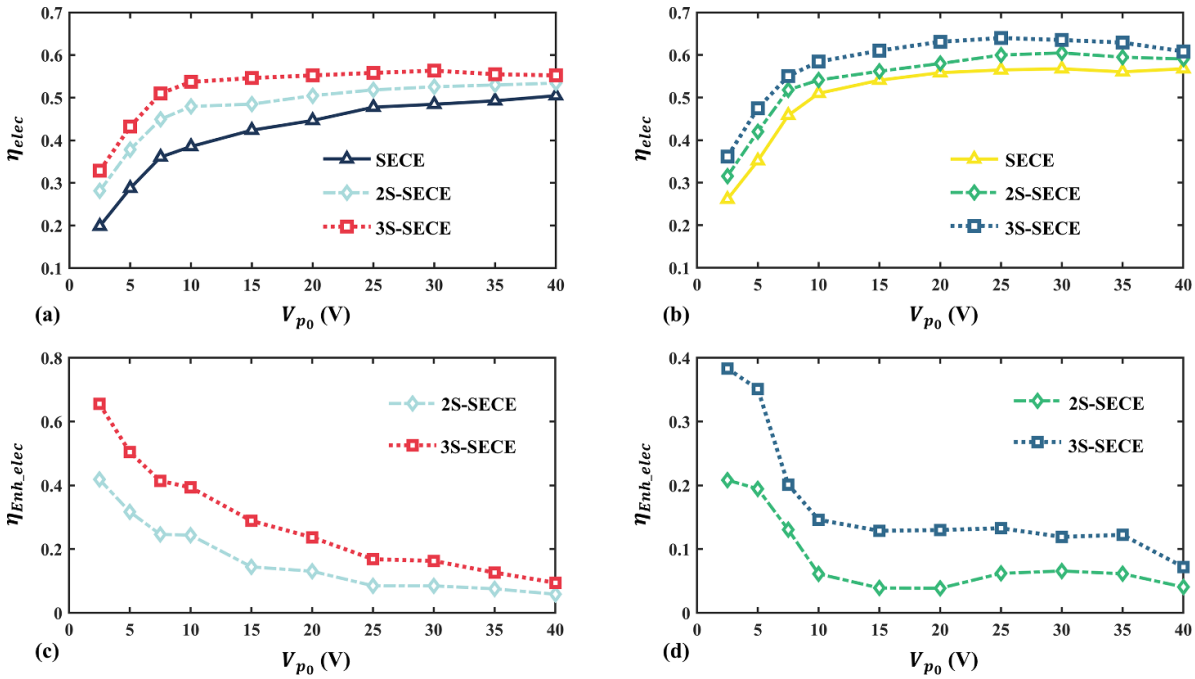

Figure 12. Overall electrical efficiency for the SECE and MS-SECE circuits and enhanced proportion for the MS-SECE circuits. (a) and (c) the results for lower circuit quality factor circuit ($Q_I \approx 3.5$); (d) and (d) the results for higher circuit quality factor circuit ($Q_I \approx 4.6$).

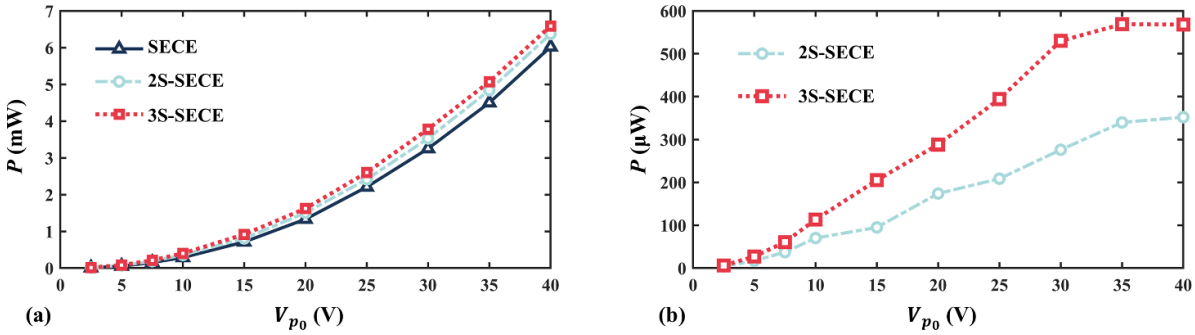

Figure 13. Harvested power and additional harvested power of the SECE and MS-SECE circuits. (a) Harvested power of the SECE, 2S-SECE and 3S-SECE circuits; (b) additional harvested power for the 2S-SECE and 3S-SECE circuits compared to the SECE circuit.

2S-SECE and 3S-SECE circuits are 173.9 μW and 288.3 μW. When V_{p_0} reaches 40 V, the values increase to 352 μW and 568 μW, respectively.

However, the use of a controller incurs additional power, therefore, the power gain and consumption should be especially considered when employing the MSEE strategy. The consumption of the low power MCU were estimated at 32.1 μW during the experiment. The longer switching time for the 2-step and 3-step cases would not significantly increase the power consumption since the total switching time is always quite smaller than the mechanical period. For the designed system, the consumption is affordable when the initial voltage is larger than a threshold voltage 5 V with 50.6 μW harvested power of the SECE circuit. The corresponding additional harvested power of the 2S-SECE and 3S-SECE circuits were measured as 17 μW and 27 μW, respectively. At 10 V initial voltage, the additional harvested power increases to 70 μW and 113 μW, which is sufficient for conducting an MPPT process for the FT-SECE circuit to further enhance the performance of the electromechanical system [40–43]. It should also be mentioned that the self-powered topology of the SECE circuit normally harvests 70% of the ideal one because of the induced phase lag [44]. The unavoidable loss may exceed the power consumption of the controller in the cases with a larger initial voltage.

Given the large capacitor for the designed piezoelectric harvester, the threshold initial voltage may increase for other designed harvesters. On the other hand, the power consumption could be further reduced by using IC solutions [45, 46]. Consequently, the effectiveness of the MSEE strategy needs to be evaluated, specifically considering the energy harvesting capacity of the mechanical structure and power consumption of the designed circuit for different cases.

6. Conclusion

In this paper, the optimal VFSs for the MS-SECE circuit are derived based on an improved theoretical model. The proposed model provides a more detailed depiction of energy flows at the synchronous instants, including the precise assessments of the components in the secondary working phase, so that the electrical efficiencies of the MS-SECE circuit can be accurately analyzed. The analytical results demonstrate that the dissipation energies caused in the secondary working phase take up a relatively smaller but non-negligible part of the total energy. It also indicates that the EC phases have little influence on the determination of the general optimal VFSs.

Based on the analysis of the electrical efficiencies, the optimal VFSs for the 2S-SECE and 3S-SECE circuits are initially identified as 1–0.6–0 and 1–0.7–0.4–0, respectively. Then, the optimal VFSs are generalized to the MS-SECE circuits by adopting a recursive approach. More importantly, the derived optimal VFSs show less dependence on the intrinsic parameters and the initial voltage, highlighting its broad applicability. The experimental results proved the accuracy of the proposed optimal VFSs and verified that the MSEE strategy was more effective under lower circuit quality factors. In comparison with the standard SECE circuit, the electrical efficiency is enhanced by 41.9% and 65.5% for the 2S-SECE and 3S-SECE circuits at a low initial voltage of 2.5 V, while the additional harvested powers are 352 μW and 568 μW at 40 V initial voltage. Moreover, the applicability of the MSEE strategy is discussed with a special focus on power gain and consumption. Overall, the proposed VFSs provide valuable guidance for enhancing electrical efficiency when designing MS-SECE circuits.

Data availability statement

All data that support the findings of this study are included within the article (and any supplementary files).

Acknowledgments

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ORCID iDs

Weiqun Liu https://orcid.org/0000-0002-0843-903X
Guobiao Hu https://orcid.org/0000-0002-1288-7564

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